AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of source/capture channels comprising one source/capture channel and remaining source/capture channels, ~~said signal source coupled to at least~~ the one source/capture channel ~~of said channels~~ being coupled to the signal source, the signal source being configured to provide ~~for providing~~ a ~~signal~~ cancellation signal to reduce ~~for reducing~~ an amplitude of a signal received by ~~said~~ the one source/capture channel, the one source/capture channel comprising:

a first combiner configured to receive a signal under test and a baseline signal and configured to provide a first combiner output signal; and

a second combiner configured to receive the first combiner output signal and configured to provide a second combiner output signal.

2. (Currently Amended) The architecture of claim 1 wherein ~~said signal source~~ the one source/capture channel further comprises a Digital-to-Analog Converter (DAC) configured to provide the baseline signal to the first combiner.

3. (Currently Amended) The architecture of claim 1, ~~wherein said system~~ further comprising ~~comprises~~ an external adjustment device coupled between ~~said~~ the source and ~~said~~ the plurality of source/capture channels.

4. (Currently Amended) The architecture of claim 1 wherein ~~at least one of said at least~~ the one source/capture channel further ~~channels~~ comprises ~~a capture~~ an Analog-to-Digital Converter (ADC) configured to receive the second combiner output signal ~~capable of receiving a signal from a device under test~~.

5. (Currently Amended) The architecture of claim 4 wherein ~~at least one of said at least one source/capture channels further comprises a~~ the second combiner is configured to receive ~~receiving~~ a cancellation signal from ~~said~~ the signal source~~, receiving a signal under test, and providing a residual signal from said cancellation signal and said signal under test to said ADC~~.

6. (Currently Amended) The architecture of claim 4 wherein the ~~at least one of said at least~~ one source/capture ~~channels~~ channel further comprises:

~~a combiner receiving a cancellation signal from said signal source, receiving a signal under test, and providing an output signal from said cancellation signal and said signal under test; and~~

an amplifier configured to receive ~~receiving said~~ the second combiner output signal ~~from said combiner~~ and configured to provide ~~providing~~ an output signal to ~~said~~ the ADC.

7. (Cancelled)

8. (Currently Amended) The architecture of claim 1 wherein ~~at least one of said at least~~ the one source/capture ~~channels~~ channel comprises:

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and~~

an amplifier configured to receive the ~~receiving said~~ second combiner output signal and configured to provide ~~providing~~ a residual signal to ~~said~~ an Analog-to-Digital Converter (ADC) ~~ADC~~.

9. (Currently Amended) The architecture of claim 4 wherein ~~at least one of said at least~~ the one source/capture channel ~~channels~~ further comprises an amplifier configured to receive

~~receiving~~ a signal from ~~said~~ the signal source and configured to provide ~~providing~~ an output to ~~a~~ the device under test.

10. (Currently Amended) The architecture of claim 4 wherein ~~at least one of said at least~~ the one source/capture channel ~~channels~~ further comprises a Digital-to-Analog (DAC) configured to provide ~~providing~~ an output to ~~a~~ the device under test.

11. (Currently Amended) The architecture of claim 1 wherein ~~said~~ the architecture is operable in a first mode wherein each channel of the plurality of source/capture channels is configured to perform a multiple capture, each channel configured substantially the same as the one source/capture channel ~~comprising:~~

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a second combiner receiving said first combiner output signal and providing a second combiner output signal; and~~

~~an amplifier receiving said second combiner output signal and providing a residual signal to said ADC~~.

12. (Currently Amended) The architecture of claim 1 wherein ~~said device~~ the architecture is operable in a second mode wherein the one source/capture channel ~~of said plurality of channels~~ is configured to perform a capture with signal cancellation,

wherein ~~said channel comprising:~~

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a~~ the second combiner is configured to receive ~~receiving~~ a cancellation signal from ~~said~~ the signal source~~, receiving said first combiner output signal and providing a second combiner output signal; and~~

~~an amplifier receiving said second combiner output signal and providing a residual signal to said ADC~~.

13. (Currently Amended) The architecture of claim 1 wherein ~~said~~ the architecture is operable in a third mode wherein each channel of ~~said~~ the plurality of source/capture channels is configured to perform a capture with signal cancellation, each channel configured substantially the same as the one source/capture channel ~~comprising:~~

wherein ~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a~~ the second combiner is configured to receive ~~receiving~~ a cancellation signal from ~~said~~ the signal source~~, receiving said first combiner output signal and providing a second combiner output signal; and~~

~~an amplifier receiving said second combiner output signal and providing a residual signal to said ADC~~.

14. (Currently Amended) The architecture of claim 12 wherein ~~said~~ in the second mode ~~further comprises~~ the remaining channels of ~~said~~ the plurality of channels are configured to perform a multiple capture, each of ~~said~~ the remaining channels comprising:

a first combiner configured to receive ~~receiving~~ a signal under test and a baseline signal, and configured to provide ~~providing~~ a first combiner output signal;

a second combiner configured to receive the ~~receiving said~~ first combiner output signal and configured to provide ~~providing~~ a second combiner output signal; and

an amplifier configured to receive the ~~receiving said~~ second combiner output signal and configured to provide ~~providing~~ a residual signal to ~~said~~ an ADC.

15. (Currently Amended) A reconfigurable testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of channels comprising one channel and remaining channels, ~~wherein said~~ the channels ~~are~~ being each configurable into a plurality of modes, each of ~~said~~ the modes providing a different level of precision from another of ~~said~~ the modes,

wherein the one channel comprises:

a first combiner configured to receive a signal under test and a baseline signal, and configured to provide a first combiner output signal; and

a second combiner configured to receive the first combiner output signal and configured to provide a second combiner output signal.

16. (Currently Amended) The architecture of claim 15 wherein ~~said~~ the plurality of modes includes a first mode wherein each channel is configured to perform a multiple capture, each channel being configured substantially the same as the one channel, the one channel further comprising:

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a second combiner receiving said first combiner output signal and providing a second combiner output signal; and~~

an amplifier receiving said second combiner output signal and providing a residual signal to an Analog-to-Digital Converter (ADC) ~~ADC~~.

17. (Currently Amended) The architecture of claim 15 wherein ~~said~~ the plurality of modes includes a second mode wherein the one channel ~~one channel of said plurality of channels~~ is configured to perform a capture with signal cancellation, ~~said~~ the one channel further comprising:

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and~~

an amplifier configured to receive the ~~receiving said~~ second combiner output signal and configured to provide ~~providing~~ a residual signal to an Analog-to-Digital Converter (ADC) ~~ADC~~.

18. (Currently Amended) The architecture of claim 15 wherein ~~said~~ the plurality of modes includes a third mode wherein each channel of ~~said~~ the plurality of channels is configured to perform a capture with signal cancellation, ~~each~~ the one channel further comprising:

~~a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;~~

~~a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and~~

an amplifier configured to receive the ~~receiving said~~ second combiner output signal and configured to provide ~~providing~~ a residual signal to an Analog-to-Digital Converter (ADC) ~~ADC~~.

19. (Currently Amended) The architecture of claim 17 wherein ~~said~~ in the second mode ~~further comprises~~ the remaining channels of ~~said~~ the plurality of channels are configured to perform a multiple capture, each of ~~said~~ the remaining channels comprising:

a first combiner configured to receive ~~receiving~~ a signal under test and a baseline signal, and configured to provide ~~providing~~ a first combiner output signal;

a second combiner configured to receive the ~~receiving said~~ first combiner output signal and configured to provide ~~providing~~ a second combiner output signal; and

an amplifier configured to receive the ~~receiving said~~ second combiner output signal and configured to provide ~~providing~~ a residual signal to an Analog-to-Digital Converter (ADC) ~~ADC~~.

20. (New) A testing architecture for automatic test equipment, comprising:

a signal source; and

source/capture channels comprising one source/capture channel and remaining source/capture channels, the one source/capture channel being coupled to the signal source, the

signal source being configured to provide a cancellation signal to reduce an amplitude of a signal received by the one source/capture channel, the one source/capture channel comprising:

a first combiner configured to receive a signal under test and a baseline signal and configured to provide a first combiner output signal;

a second combiner configured to receive the first combiner output signal and configured to provide a second combiner output signal;

an Analog-to-Digital Converter (ADC) configured to receive the second combiner output signal; and

a Digital-to-Analog Converter (DAC) configured to provide the baseline signal to the first combiner.

21. (New) The architecture of claim 20, further comprising:

a first amplifier configured to receive the second combiner output signal and configured to provide an output signal to the ADC; and

a second amplifier configured to receive a signal from the signal source and configured to provide an output to the device under test.